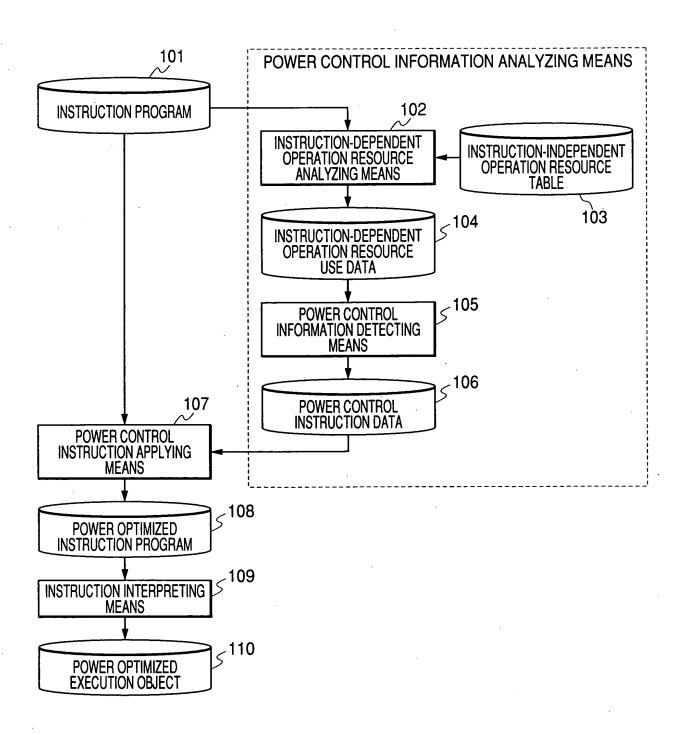


FIG. 1



	202 OPERATION RESOURCE														
MOITAGE OF A POST MONTH	MEMORY READ OPERATION	MEMORY WRITE OPERATION	CALCULATOR A OPERATION	CALCULATOR B OPERATION	BRANCH UNIT A OPERATION	BLOCK A OPERATION	BLOCK B OPERATION	BLOCK C OPERATION	PERIPHERAL INTERFACE A OPERATION	PARALLEL INSTRUCTION DECODE UNIT	DATA REGISTER R0 TO R15	DATA REGISTER R16 TO R31	ADDRESS CALCULATION UNIT	THRESHOLD VALUE UNIT	
	0	0	1	0	0	0	0	0	0	0	1	1	0	0	
	1	0	1	0	0	1	0	0	0	0	1	1	1	0 0 1	
	0	0	1	0	0	0	0	0	0	0	1	0	0	1	
	1	0	0	0	0	1	0	0	0	0	0	0	0	0	
	1	0	1	0	0	1	0	0	0	1	1	1	0	0	
	0	1	0	0	0	1	1	0	0	0	1	0	0	0	
	0	0	0	1	0	0	0	0	0	0	1	1	0	0 0 0 0	
	0	0	0	0	0	0	0	0	1	0	0	0	1	1	
L	0	0	0	0	1	0	0	0	0	0	1	0	0	0	
	0	0	0	0	1	0	0	1	0	0	0	0	0	1	
					:										

201 INSTRUCTION MODE

\sim	
ADD	Rx, Ry, Rz
ADD	Rx, MEMy, MEMz
ADD	Rx, Ry, imm
LD	Ry, MEMy
LD	Ra, MEMy, ADD Rx, Ry, Rz
STR	Ra, MEMy
MUL	Rx, Ry, Rz
10	ADDR
JUMP	Rx
LOOP	N

INSTRUCTION-INDEPENDENT OPERATION RESOURCE TABLE

MEMORY READ OPERATION
MEMORY WRITE OPERATION
CALCULATOR A OPERATION
CALCULATOR B OPERATION
BRANCH UNIT A OPERATION
BLOCK A OPERATION
BLOCK C OPERATION
PERIPHERAL INTERFACE A OPERATION
PARALLEL INSTRUCTION DECODE UNIT
DATA REGISTER R0 TO R15
DATA REGISTER R16 TO R31

ADDRESS CALCULATION UNIT

THRESHOLD VALUE UNIT

302

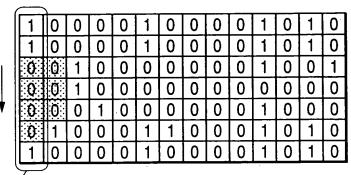
	301
LD	R1, Mem(A0)
LD	R1, Mem(A1)
SUB	R0, R1, 0xffff
ADD	R2, R5, R7
MUL	R3, R0, R2
STR	Mem(A4), R3
LD	R4, Mem(A5)

1	0	0	0	0	1	0	0	0	0	1	0		0
1	0	0	0	0	1	0	0	0	0	1	0		0
0	0	1	0	0	0	0	0	0	0		0	0	:1
0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	0		0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	1	1	0	0	0	1	0		0
1	0	0	0	0		0	0	0	0		0		0

INSTRUCTION-INDEPENDENT OPERATION RESOURCE USE DATA

MEMORY READ OPERATION
MEMORY WRITE OPERATION
CALCULATOR A OPERATION
CALCULATOR B OPERATION
BRANCH UNIT A OPERATION
BLOCK A OPERATION
BLOCK COPERATION
PERIPHERAL INTERFACE A OPERATION
PARALLEL INSTRUCTION DECODE UNIT
DATA REGISTER R16 TO R15
DATA REGISTER R16 TO R31

LD R1, Mem(A0) LD R1, Mem(A1) SUB R0, R1, 0xffff ADD R2, R5, R7 MUL R3, R0, R2 STR Mem(A4), R3 LD R4, Mem(A5)



LD.	R1, Mem(A0)
LD	R1, Mem(A1)
SETPCR	#Memory_Read_Stop
SUB	R0, R1, 0xffff
ADD	R2, R5, R7
MUL	R3, R0, R2
STR	Mem(A4), R3
CLR PCR	#Memory_Read_Stop
LD	R4, Mem(A5)

POWER CONTROLLING SUBJECT 1	POWER CONTROLLING SUBJECT 2	POWER CONTROLLING SUBJECT 3	POWER CONTROLLING SUBJECT 4	 POWER CONTROLLING SUBJECT n
0	1	0	0	0

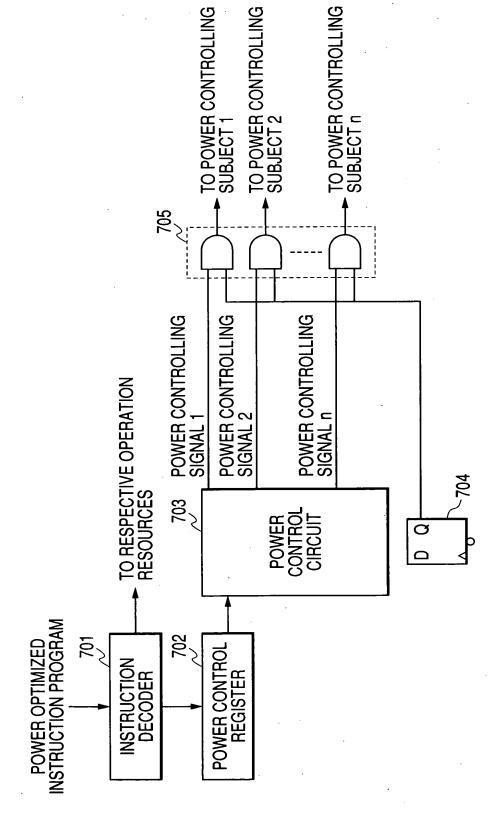


FIG. 7

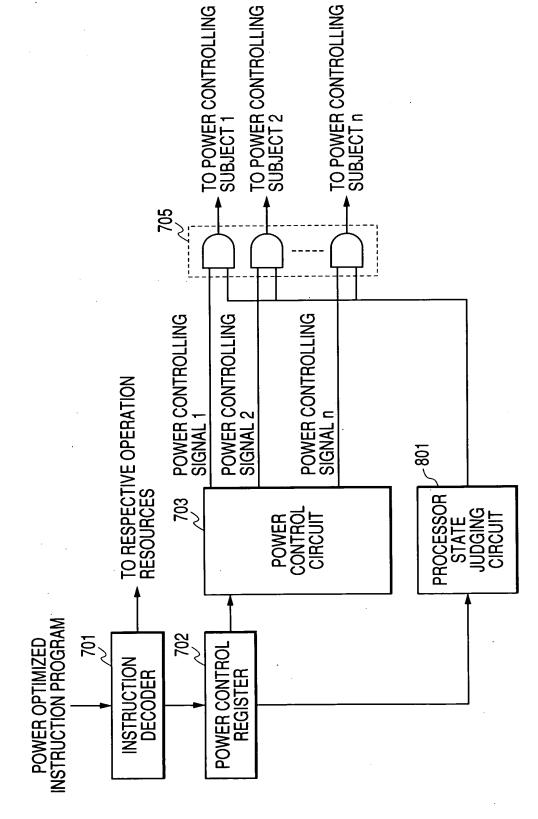


FIG. 8

PROGRAM ID	POWER CONTROL FUNCTION ON/OFF
ID1	ON
ID2	ON
ID3	OFF
ID4	ON

```
data_a = data_b*1.75;
data_c = func_calc_d(in1, in2, in3);

if(cond_k==1) {adrs1 = adrs1+8;}

#pragma POWER_CONT_ON_Level1
for(i=0; i<256; i++) {
   out_sum = out_sum*data_c[adrs1]
}
#pragma POWER_CONT_OFF

if(out_sum>24) {adrs1 = adrs1+32;}
```

LEVEL	CONTROL CONTENT
LEVEL 0	ONLY OPERATION RESOURCE WHICH CAN BE STOPPED IS DETECTED BY REPLACING INSTRUCTIONS
LEVEL 1	OPERATION RESOURCE WHICH IS NOT ACTUATED FOR 10, OR MORE SECTIONS IS DETECTED
LEVEL 2	OPERATION RESOURCE WHICH IS NOT ACTUATED FOR 5, OR MORE SECTIONS IS DETECTED
LEVEL 3	OPERATION RESOURCE WHICH IS NOT ACTUATED FOR 3, OR MORE SECTIONS IS DETECTED

FIG. 12

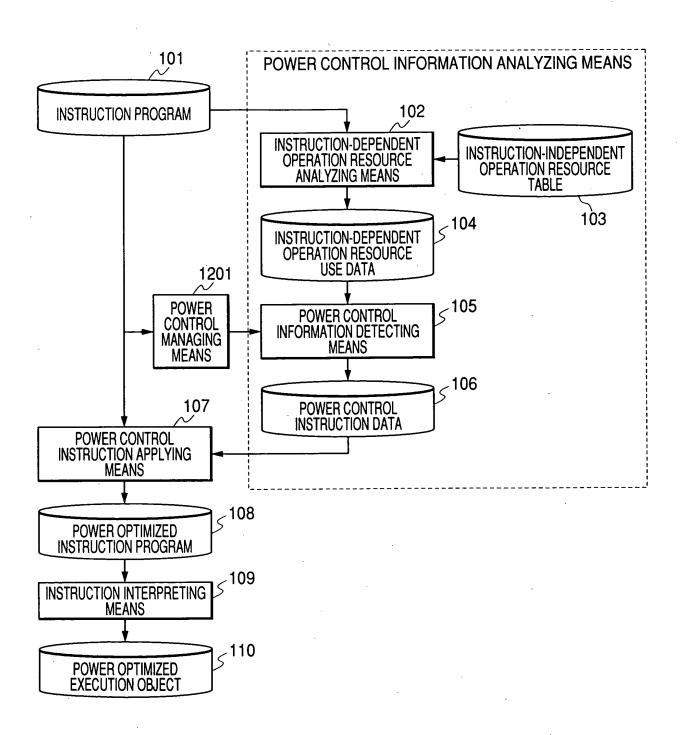
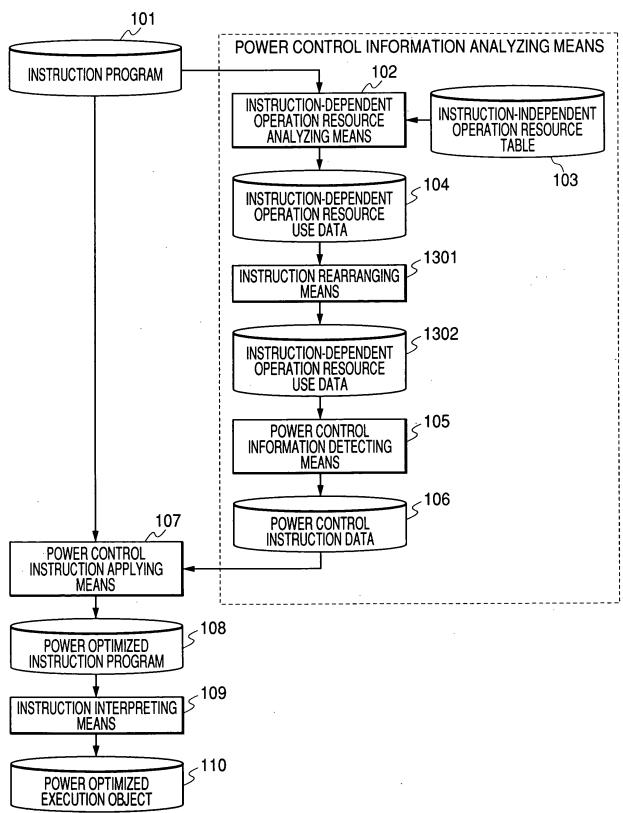


FIG. 13



MEMORY READ OPERATION
MEMORY WRITE OPERATION
CALCULATOR A OPERATION
CALCULATOR B OPERATION
BRANCH UNIT A OPERATION
BLOCK A OPERATION
BLOCK B OPERATION
BLOCK C OPERATION
PERIPHERAL INTERFACE A OPERATION
PARALLEL INSTRUCTION DECODE UNIT

MOV R0, 0X00aa ADD R5, R5, R0 LD R1, Mem(A1) SUB R0, R1, 0X0fff LD R7, Mem(A0) ADD R2, R5, R7 MUL R3, R0, R2 STR Mem(A4), R3

0	0	1	0	0	0	0	0	0	0	1	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	1	0	1	0
0	0	1	0	0	0	0	0	0	0	T	0	0	1
1	0	0	0	0	1	0	0	0	0	1	0	1	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	1	1	0	0	0	1	0	1	0

DATA REGISTER R16 TO R31

DATA REGISTER R0 TO R15

FIG. 15

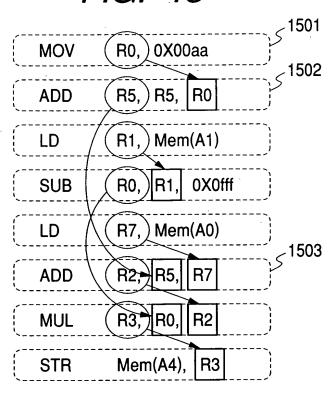
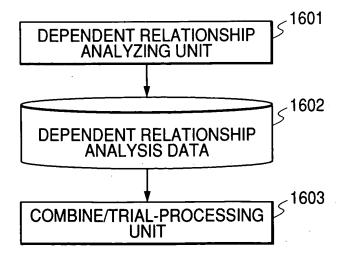


FIG. 16

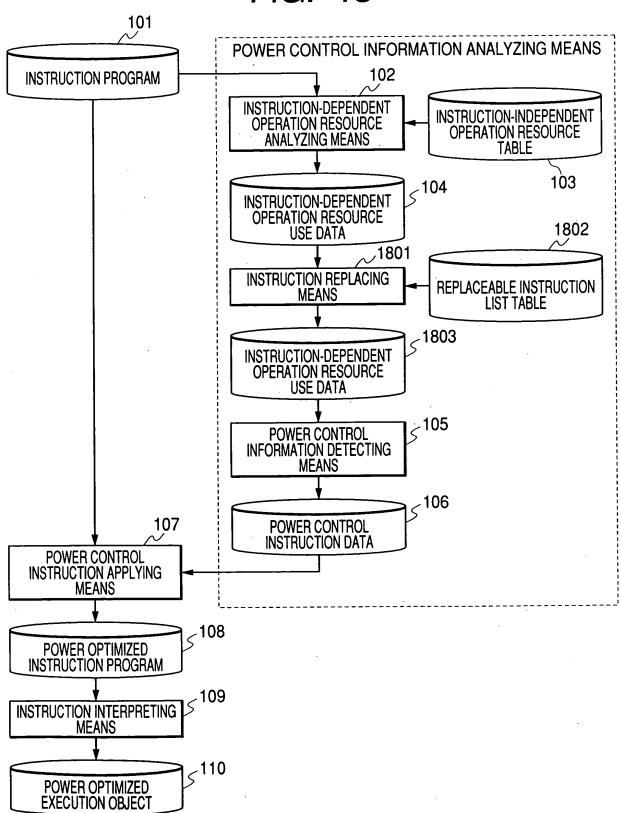


MEMORY READ OPERATION
MEMORY WRITE OPERATION
CALCULATOR A OPERATION
CALCULATOR B OPERATION
BRANCH UNIT A OPERATION
BLOCK A OPERATION
BLOCK COPERATION
BLOCK COPERATION
PERIPHERAL INTERFACE A OPERATION
PARALLEL INSTRUCTION DECODE UNIT
DATA REGISTER R0 TO R15
DATA REGISTER R16 TO R31

LD R1, Mem(A1) R7, Mem(A0) LD MOV R0, 0X00aa **ADD** R5, R5, R0 **SUB** R0, R1, 0X0fff **ADD** R2, R5, R7 MUL R3, R0, R2 Mem(A4), R3 **STR**

1	0	0	0	0	1	0	0	0	0	1	0	1	0
1	0	0	0	0	1	0	0	0	0	7	0	1	0
0	0	1	0	0	0	0	0	0	0	1	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	Ω	1	0	0	0	0	0	0	0	1	Ö	0	1
0	0	1	0	0	0	0	0.	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	1	1	0	0	0	1	0	1	0

FIG. 18



MEMORY READ OPERATION
MEMORY WRITE OPERATION
SHIFTER OPERATION
BULTIPLIER OPERATION
BLOCK A OPERATION
BLOCK B OPERATION
BLOCK C OPERATION
PERIPHERAL INTERFACE A OPERATION
PARALLEL INSTRUCTION DECODE UNIT
DATA REGISTER R0 TO R15
DATA REGISTER R16 TO R31

Mem(A2), R9 STR MUL R3, R0, 0x0002 LD R1, Mem(A1) R5, R7, 0x0004 MUL **SUB** R0, R1, 0x0fff **ADD** R2, R5, R7 R3, R0, R2 **MUL** Mem(A4), R3 **STR**

0	0	1	0.	0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	1	0	0	0	0	1	0	1	0
0	0	0	1	0	0	0	0	0	0	1	0	0	0
0	0	1	0	0	.0	0	0	0	0	1	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	1	0	0	0
0	1	0	Q	0	1	1	0	0	0	1	0	1	0

MEMORY READ OPERATION
MEMORY WRITE OPERATION
SHIFTER OPERATION
MULTIPLIER OPERATION
BRANCH UNIT A OPERATION
BLOCK A OPERATION
BLOCK B OPERATION
BLOCK C OPERATION
PERIPHERAL INTERFACE A OPERATION
PARALLEL INSTRUCTION DECODE UNIT

STR Mem(A2), R9
SFT R3, R0, 0x0001
LD R1, Mem(A1)
SFT R5, R7, 0x0002
SUB R0, R1, 0x0fff
ADD R2, R5, R7
MUL R3, R0, R2
STR Mem(A4), R3

0	0	1	0	0	0	0	0	0	0	1	0	0	1
0	0	1	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	1	0	0	0	0	1	0	1	0
0	0	1	0	0	0	0	0	0	0	1	0	0	0
0	0	1	0	0	0	0	0	0	0	1	0	0	0
0	0	1	0	0	0	0	0	9	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	1	1	0	0	0	1	0	1	0

DATA REGISTER R16 TO R31

DATA REGISTER R0 TO R15

